UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,430	04/09/2004	Robert E. Cypher	5181-95901	1241

35690 7590 11/16/2006

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX 78701

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,430	CYPHER, ROBERT E.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,14,17-21 and 30* is/are rejected.

7)☒ Claim(s) *6-13,15,16,22-29,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the response filed 8/23/2006. Claims 1-32 remain pending.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

The Examiner has applied new grounds of rejection to the claims as well as maintained the previous rejections as set forth below. As such, this action has been made Non-Final.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Arguments

Applicant's arguments, see pages 9-11 of the current response with respect to the rejection(s) of claim(s) 1-32 under 35 U.S.C. §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection under §103(a) is made in view of Dieffenderfer et al. in view of Steiss et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,14,17-21, and 30, are rejected under 35 U.S.C. 103(a) as being unpatentable Dieffenderfer et al. (U.S. Patent Application Publication No. 2004/0186964) in view of Steiss et al. (U.S. Patent No. 6,895,493).

As per claims 1 and 17, Dieffenderfer teaches a **storage** (register group containing bit indications for each cache address as taught in ¶21) **including a plurality of entries to store corresponding snoop filter indications** (each of a group of single bit indications containing a logical high bit or a logical low bit - ¶21) and **a cache controller** (any of the non-requesting snoop controllers 10b-10n of figure 1) **configured to receive a transaction request including an address** (refer to the snoop transaction shown in figure 3) **and to generate an index for accessing said storage** (register) **by performing a hash function on the address.** Dieffenderfer teaches that a variety of techniques may be used to determine whether a snoop should be performed on the cache (meaning that an entry in the cache likely exists) (¶21), such as using an address of a transaction request (¶24), but does not specifically teach using a hash function on the address to generate an index, which is then used to determine if the cache should be snooped. Steiss teachs in [2/16-28] and [3/21-35] that using a hashing function on an incoming requests address reduces the power required to make a comparison since the hashed address value (i.e. the index) is smaller and less comparison is needed. In addition, using a

hashed value of an incoming address that produces a smaller index than the incoming request's address, allows for a faster comparison , thereby able to reduce the latency required when determining whether a snoop request should be performed with the system of Dieffenderfer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the snoop filtering system of Dieffenderfer with the hashing teaching of Steiss in order to have reduced the latency required when filtering snoop addresses of incoming requests and also to have reduced the power needed when comparing the addresses of the incoming requests and the register entries (¶21of Dieffenderfer).

Further, Dieffenderfer teaches **said cache controller further configured to selectively generate a snoop request operation** (figure 2, steps 45-46) **to said cache memory** (step 46) **for said transaction request dependent upon a snoop filter indication** (dependent upon the indication stored in the register for the respective address of the incoming request - ¶21) **stored in said storage** (register) **that corresponds to said address**. Refer to ¶21.

As per claims 2 and 18, Dieffenderfer teaches **said cache controller is configured to generate said snoop response to said cache memory for said transaction request if said snoop filter indication is a value indicative that a cache line** (logic high - '1' - stored in the respective entry of the register - ¶21) **corresponding to said address was stored within said cache memory**. The address of an incoming request may be used to filter snoops as taught in ¶24.

As per claims 3 and 19, Dieffenderfer teaches **said cache controller is configured to ignore said transaction request if said snoop filter indication is a value indicative that a cache line corresponding to said address is not stored within said cache memory** in ¶21. A

'0' (logic low) in a corresponding register entry indicates that the incoming request not does have an associated entry within the cache.

As per claims 4 and 20, Dieffenderfer teaches **wherein during a first mode of operation** (which the Examiner is considering to be normal cache directory operation as Dieffenderfer does not teach multiple modes of operation) **and in response to a cache memory access, said cache controller is configured to store said snoop filter indication** (corresponding single bit entry of the register) **in an entry of said storage** (register) **having an index** (which the Examiner is considering to be the result of the hashing algorithm for a given requested address as taught by Steiss) **equal to the hash value of an address associated with said cache line** as at one point, prior to the requested data being stored in the cache, it is necessarily inherent that the associated entry of the register corresponding with the cache line stored in the cache have a logic high ('1') indication stored therein, thereby indicating that the cache line may be stored in the cache (and accessed - figure 2, steps 45-46.

As per claims 5 and 21, Dieffenderfer teaches **a second storage** (register memory of another bus master, 10c for example) **including a plurality of entries configured to store second snoop filter indications** as each bus master 10 may have its own register of bit entries - ¶21.

As per claims 14 and 30, Dieffenderfer teaches **said cache memory including a plurality of portions** (cache lines) **and each portion of said cache memory corresponds to a respective portion** (particular single bit entry of the register) **of said plurality of entries of said storage** (entire register) - ¶21. It can be seen that the entries of the register correspond to an entry portion of the cache (cachelines) as for each incoming memory request, a lookup is

performed in the register to determine whether to snoop the respective cache line - steps 45-46 of figure 2.

Allowable Subject Matter

Claims 6-13,15,16,22-29,31, and 32, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claims 6 and 22, the prior art of record does not specifically teach **a second mode of operation,** where when in the second mode, **the cache controller is further configured to selectively generate a snoop operation to said cache memory for said transaction request dependent upon a second snoop filter indication stored in said second storage that corresponds to said address.** Specifically, Dieffenderfer does not teach a second mode using a second register to determine if a specific set of data is contained in the cache.

As per claims 15 and 31, the prior art of record does not specifically teach **generating a snoop operation to a given one of said portions of said cache memory if said corresponding respective portion of said plurality of entries of said storage is populated with a predetermined number of said snoop filter indications.** Specifically, Dieffenderfer only teaches a single snoop filter indications for each entry of the cache as discussed.

Claims 7-13,16,23-29, and 32 are allowable over the prior art of record as being dependent upon allowable base claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SMT

Shane M. Thomas

PIERRE BATAILLE
PRIMARY EXAMINER
11/13/06